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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/994,936	11/28/2001	Sadashige Sugiura	60188-121	7332

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EXAMINER	
HU, SHOUXIANG	

ART UNIT	PAPER NUMBER
2811	

DATE MAILED: 04/16/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/994,936	SUGIURA ET AL.	
	Examiner	Art Unit	
	Shouxiang Hu	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE ____ MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 January 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-12,19 and 20* is/are pending in the application.

4a) Of the above claim(s) *2 and 6-12* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3-5,19 and 20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *16 January 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Priority

1. This application claims priority under 35 U.S.C. 119 based on priority application serial No. 2000-360526, filed on November 28, 2000, in Japan.

Election/Restriction

2. Claims 2 and 6-12 have been withdrawn from further consideration pursuant to 37 CFR 1.142(b) as being drawn to a nonelected invention, in view of the previous office action, there being no allowable generic or linking claim. Election was made **without** traverse in Paper No. 9.

Accordingly, claims 1-12, 19 and 20 are pending in this application; and claims 1, 3-5, 19 and 20 remain active in this Office action.

Drawings

3. The new corrected drawings of Figs. 3A-3D were received on January 16, 2004. These drawings are approved.

Claim Objections

4. Claims 4 and 5 are objected to because of the following informalities and/or defects:

Claims 4 and 5 each recite the terms of "the opposite polarity", but fail to clarify with respect to what polarity it is meant to be opposite to.

Appropriate correction is required.

Claim Rejections - 35 USC § 112

5. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

6. Claims 3, 19 and 20 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

Claim 3 recites the subject matters that the test pad is a portion of the recited wire(s). However, according to the specification and drawings (especially see Figs. 3A-3D), the test pad (33 or 34) is much wider than the wire (or wires; 31 and/or 32); and they are located at different locations. Apparently, the test pads therein is not a portion of the wires as the test pads therein are not wire-shaped, even through they are connected to the wires and might be made from a portion of layer same as the wiring layers.

Claims 19 and 20 each recite the subject matters that the recited semiconductor device further comprises at least one test pin. However, the original disclosure lacks an

adequate description regarding how the recited pin could be formed in the recited device, given the fact that a test pin normally is a part of a test instrument for probing/testing a semiconductor device through landing such test ping on the test pad, instead of being a part of the semiconductor device.

Claim Rejections - 35 USC § 102

7. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1, 3, 19 and 20, insofar as being in compliance with 35 U.S.C. 112, are rejected under 35 U.S.C. 102(b) as being anticipated by Nakanishi et al. ("Nakanishi"; US 5,110,664).

Nakanishi discloses a semiconductor device (See Fig. 1), comprising: a semiconductor wiring substrate (17, 37 and 18) including a plurality of wires (13 and 29); a IC chip (1), which is regarded here as inherently having intellectual property and including a circuit having semiconductor device elements arranged therein; and at least one test pad (3) connected to at least one of the wires of the semiconductor wiring substrate. The test pad (3) in Nakanishi is naturally capable of functioning as a test pad for testing an electrical connection between the circuit of the chip and the wires, since it is a test pad and is electrically connected to both of the circuit and the wires. Furthermore, it is noted that the limitation of "for testing an electrical connection

between the circuit of the chip IP and the wires" is an intended-use limitation.However, a recitation of the intended use of the claimed invention must result in a structural difference between the claimed invention and the prior art in order to patentably distinguish the claimed invention from the prior art. If the prior art structure is capable of performing the intended use, then it meets the claim. In a claim drawn to a process of making, the intended use must result in a manipulative difference as compared to the prior art. See *In re Casey*, 152 USPQ 235 (CCPA 1967) and *In re Otto*, 136 USPQ 458, 459 (CCPA 1963).

Regarding claim 3, insofar as being in compliance with 35 U.S.C. 112, the test pad in Nakanishi is a portion of a circuit that includes at least one of the wires that is exposed on a surface of the semiconductor wiring substrate.

Regarding claims 19 and 20, insofar as being in compliance with 35 U.S.C. 112, it is noted that the limitation regarding "for applying" a voltage is an intended-use limitation; and that the test pad in Nakanishi is naturally capable of receiving a test pin for applying or detecting a voltage thereon.

Claim Rejections - 35 USC § 103

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 4 and 5, insofar as being in compliance with 35 U.S.C. 112 and as being best understood in view of the above claim objections, are rejected under 35 U.S.C. 103(a) as being unpatentable over Nakanishi et al. ("Nakanishi"; US 5,110,664) in view of Voldman (US 5,625,280).

The disclosure of Nakanishi is discussed as applied to clams 1 and 3 above.

Nakanishi does not expressly disclose that the circuit in the chip can have a diode connected to a power supply line and a node and then to two test pads. However, one of ordinary skill in the art would readily recognize that a circuit in a chip can be protected by a diode, as evidenced in Voldman. Voldman (see Figs. 1-3, and col. 5, lines 19-24) teaches to protect a circuit from ESD damages by connecting a protection diode (27 or 28) between a node (26) and a line (a power supply line10; or a ground line 13), wherein the node and the line are connected respectively to pads (26) and 11 (or the bottom left one).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the pad-connected protection diode of Voldman into the device of Nakanishi, so that a semiconductor device with better chip protection would be obtained. In addition, it is noted that the term regarding "through which a forward current flows" when a voltage is applied is an intended-use limitation; and, such a diode in the collectively taught device would be naturally capable of carrying a forward current when a voltage with an appropriate polarity is applied to the power supply line or the ground line.

Response to Arguments

9. Applicant's arguments filed on 5/15/03 have been fully considered but they are not persuasive.

Applicant's main arguments include: (A) Nakanishi does not anticipate the claimed invention, because Nakanishi is silent as to how the test pad 3 would be used to test electrical connections between the substrate wiring and the chip; and (B) There is no suggestion to combine the applied references.

With respect to applicant's Argument A above, it is noted that the test pad 3 in Nakanishi is a test pad that is electrically connected to the circuit in the chip through at least one of the wirings (13) in the substrate; and such a test pad is intended to test the electrical properties of the circuit in the chip through the wiring(s) (see particularly Fig. 1, and col. 6, lines 31-35). Accordingly, the connection testing (a test of the electrical connection between the circuit of the chip and the wirings) would be the least such an electrical test pad has to be able to function, otherwise the test pad would not be able to test anything else about the chip. Therefore, the test pad 3 in Nakanishi is naturally capable of testing the electrical connection between the circuit of the chip and the wires. Furthermore, it is noted that the limitation of "for testing an electrical connection between the circuit of the chip IP and the wires" is an intended-use limitation. However, a recitation of the intended use of the claimed invention must result in a structural difference between the claimed invention and the prior art in order to patentably distinguish the claimed invention from the prior art. If the prior art structure is capable of performing the intended use, then it meets the claim. In a claim drawn to a process of

making, the intended use must result in a manipulative difference as compared to the prior art. See *In re Casey*, 152 USPQ 235 (CCPA 1967) and *In re Otto*, 136 USPQ 458, 459 (CCPA 1963). In this case, the structure of Nakanishi is naturally capable of testing the electrical connection between the circuit of the chip and the wires, it thus anticipates the instant invention as defined at least in claims 1.

Regarding applicant's Argument B that there is no suggestion to combine the references, the examiner recognizes that obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either in the references themselves or in the knowledge generally available to one of ordinary skill in the art. See *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988)and *In re Jones*, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992). In this case, although Nakanishi does not expressly disclose that the circuit in the chip can have a diode connected to a power supply line and a node and then to two test pads, one of ordinary skill in the art would readily recognize that a circuit in a chip can be protected by such a diode connection. And, such knowledge and desirability are generally available to one of ordinary skill in the art, as evidenced in Voldman. Voldman (see Figs. 1-3, and col. 5, lines 19-24) teaches to protect a circuit from ESD damages by connecting a protection diode (27 or 28) between a node (26) and a line (a power supply line10; or a ground line 13), wherein the node and the line are connected respectively to pads (26) and 11 (or the bottom left one). It would therefore well within the ordinary skill in the art at the time the invention was made to incorporate the pad-connected protection diode of Voldman

into the device of Nakanishi for forming a semiconductor device with better chip protection. Moreover, it is noted that ESD concerns are common in the art for semiconductor devices; and applicant's arguments fail to persuasively show why they should not be concerned in the semiconductor device of Nakanishi.

Responses to applicant's other arguments are incorporated into the claim rejections set forth above in this Office action.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Shouxiang Hu whose telephone number is 571-272-1654. The examiner can normally be reached on Monday through Thursday, 7:30 AM to 6:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie C. Lee can be reached on 571-272-1732. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should

you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

SH
April 13, 2004

SHOUXIANG HU
PRIMARY EXAMINER